REMARKS

This responds to the Office Action mailed on October 28, 2005. Claims 1, 6, 9, 15, 17, 24, 58, 64, 72 and 75 are amended, no claims are canceled, and no claims are added. Thus, claims 1-7, 9-28 and 58-77 remain pending in this application.

Claims 1, 6, 9, 15, 17, 24, 58, 64, 72 and 75 have been amended to correct typographical errors and to remove extra spaces. Applicant respectfully submits that no new matter was added in making these amendments to the claims.

First §103 Rejection of the Claims

Claims 1-7 and 9-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chern (U.S. 6,287,921) in view of Ho et al. (U.S. 5,674,775, "Ho"). Applicant respectfully traverses the rejection for as least the following reasons.

Independent claims 1, 6, 9, 15, 17, 24 and 28 each refer to an apparatus having reduced transistor leakage attributes. Applicant is unable to find in the cited portions of Chern and Ho either a showing or a fair suggestion of an apparatus having reduced transistor leakage attributes. For example, Chern (at column 2 lines 34-41 in context with column 1 lines 48-53) refers to providing precise threshold voltages by preventing diffusion of the threshold adjustment dopants used to balance a pair of PMOS and NMOS transistors in CMOS circuits, but this portion of Chern neither mentions nor fairly suggests reducing or preventing transistor leakage. Likewise, Ho (at column 3, lines 1-4) refers to trench formation to allow proper formation of gate oxide around the trench and to reduce parasitic field FET problems, but this portion of Ho neither mentions nor fairly suggests reducing or preventing transistor leakage.

Additionally, Applicant respectfully asserts that there is no objective evidence in either reference to support the combination of the references. Applicant is unable to find a suggestion in either Chern or Ho to combine the threshold voltage adjustment method of Chern with the isolation trench of Ho.

With respect to independent claim 1, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus including a dopant in the implant region having the same dopant type as the substrate type whereby the

threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 1. Claims 2-5 depend, either directly or indirectly, on independent claim 1, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 1.

With respect to independent claim 6, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus including a dopant in the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 6. Claim 7 depends on claim 6, and is believed to be allowable for the reasons provided with respect to claim 6.

With respect to independent claim 9, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus including a dopant in the implant region and the substrate at the at least one trench wall region wherein the implant region has the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 9. Claims 10-14 depend, either directly or indirectly, on independent claim 9, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 9.

With respect to independent claim 15, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus including a dopant in the implant and migration regions region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 15. Claim 16 depends on claim 15, and is believed to be allowable for the reasons provided with respect to claim 15.

With respect to independent claim 17, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus including a dopant in the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 17. Claims 18-23 depend, either directly or indirectly, on independent claim 17, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 17.

With respect to independent claim 24, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an apparatus having reduced transistor leakage attributes including a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform, as recited in claim 24. Claims 25-27 depend, either directly or indirectly, on independent claim 24, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 24.

With respect to independent claim 28, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of a transistor structure having reduced transistor leakage attributes including a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform, as recited in claim 28.

Reconsideration of the rejections and allowance of claims 1-7 and 9-28 are respectfully solicited.

Second §103 Rejection of the Claims

Claims 58-77 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chern and Ho in view of Salling et al. (U.S. 6,515,889, "Salling"). Applicant respectfully traverses the rejection for as least the following reasons.

As stated above, Applicant respectfully asserts that Chern and Ho do not disclose apparatus having reduced leakage attributes as recited. Applicant respectfully submits that the deficiencies in the rejections with respect to Chern and Ho discussed above are not overcome by combination with the cited portions of Salling. In addition, Applicant respectfully asserts that there is no objective evidence in any of the references to support the combination of the references. Applicant is unable to find a suggestion in Chern, Ho or Salling to combine the threshold voltage adjustment method of Chern with the isolation trench of Ho and the depletion-mode ferroelectric memory cells of Salling.

With respect to independent claim 58, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an electronic system having a memory device including a dopant in the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 58. Claims 59-63 depend, either directly or indirectly, on independent claim 58, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 58.

With respect to independent claim 64, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an electronic system having a memory device including a dopant in the implant region and the substrate at the at least one trench wall, the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 64. Claims 65-71 depend, either directly or indirectly, on independent claim 64, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 64.

With respect to independent claim 72, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an electronic system having a memory device including a dopant in the implant region and the migration region, the implant region having the same dopant type as the substrate type whereby the threshold voltage in the implant region is approximately equal to or greater than the threshold voltage on the portion of the substrate and whereby the pull back distance defines a width of the implant region which is approximately uniform around the process stack, as recited in claim 72. Claims 73-74 depend, either directly or indirectly, on independent claim 72, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 72.

With respect to independent claim 75, Applicant is unable to find among other things in the cited portions of the cited references, a teaching or fair suggestion of an electronic system including a memory device having reduced transistor leakage attributes, including a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the corner region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the transistor structure, the threshold voltage of the central area of the substrate being about substantially uniform, as recited in claim 75. Claims 76-77 depend, either directly or indirectly, on independent claim 75, and are believed to be in condition for allowance at least for the reasons provided with respect to claim 75.

Reconsideration of the rejections and allowance of claims 58-77 are respectfully solicited.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Daniel Mertes at (715) 824-5144 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of 2006.

KATE GANNON

Name

Signature